Amendments of the Claims

This listing of claims will replace all prior versions and listings of claims in this application:

Listing of Claims

1. (currently amended) Digital signal processing (DSP) circuitry that independently processes a plurality of multi-channel data signals, comprising:

a plurality of columns of registers, each said column comprising a single input, an output and a plurality of registers arranged in serial as a sequence of registers, wherein the single input is coupled to a register of the plurality of registers that is positioned first in the sequence of registers; and

interconnection circuitry for allowing ~~successive~~ a first channel ~~channels~~ of said plurality of multi-channel data signals to be selectively shifted, at the same time, through said plurality of registers in ~~each~~ a first and a second of said columns ~~and to also be selectively shifted through a plurality of registers in at least one other of said plurality of columns~~, wherein said interconnection circuitry:

allows a value at the single input of each column to be selectively routed to any said register in said respective column by bypassing any register or registers that precede said register in said respective column, and

allows the output of the first column to be selectively shifted through said plurality of registers in the

second column instead of the first channel that is received by the first and second columns at the same time.

2. (currently amended) The circuitry of claim 1, further comprising utilization circuitry for operating on a first piece of data output by a register in [[a]] the first of said columns and a second piece of data output by a register in [[a]] the second of said columns, wherein the first and second pieces of data each corresponds to [[a]] the first channel of the plurality of multi-channel data signals.

3. (original) The circuitry of claim 2, wherein said utilization circuitry comprises circuitry selected from the group consisting of adder circuitries, multiplier circuitries, and a combination thereof.

4. (original) The circuitry of claim 1, wherein the interconnection circuitry comprises:

a multiplexer circuit associated with each register in each said column.

5. (original) The circuitry of claim 1, wherein said interconnection circuitry allows successive data signals to be shifted to as many different said plurality of columns as needed such that the output of each of those columns is used as an input to a finite impulse response filter function.

6. (currently amended) The circuitry of claim 5, wherein a respective register in each of those columns provides a respective piece of the output data used as the input to the filter function, wherein each respective piece of the output data corresponds to [[a]] <u>the</u> first channel of the plurality of multi-channel data signals.

7. (original) The circuitry of claim 1, wherein said interconnection circuitry can selectively route data signals past one or more of said registers in each said column.

8. (previously presented) The circuitry of claim 1 wherein said circuitry is mounted on a programmable logic device.

9. (original) The programmable logic device defined in claim 8 further comprising:

routing circuitry for selectively supplying signals to and receiving signals from the DSP circuitry.

10. (original) The programmable logic device defined in claim 9 further comprising:

programmable logic circuitry connected to the routing circuitry.

11. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

a programmable logic device as defined in claim 8 coupled to the processing circuitry and the memory.

12. (previously presented) The circuitry of claim 8 wherein said circuitry is mounted on a printed circuit board.

13. (original) The printed circuit board defined in claim 12 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

14. (original) The printed circuit board defined in claim 12 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

15. (currently amended) A programmable logic device (PLD), comprising:

digital signal processing (DSP) circuitry that supports multiple channels of data being transmitted on the same carrier, said DSP circuitry comprising:

tap delay line circuitry that comprises:

first and second columns of registers for selectively registering, at the same time, the same data of ~~each of~~ a first of the multiple channels such that the data of each channel is not mixed with the data of any other channel,

wherein the registers are arranged in serial as a sequence of registers, ~~wherein the tap delay line circuitry comprises:~~

a single input coupled to a register of the plurality of registers that is positioned first in the sequence of registers; and

interconnection circuitry that:

allows a value received at the single input to be selectively routed to any register of said registers in said tap delay line circuitry by bypassing any register or registers that precede said register in said tap delay line circuitry, and

allows an output of the first column to be selectively registered in said plurality of registers in the second column instead of the data of the first channel that is received by the first and second columns at the same time; and

utilization circuitry that performs a function on data received from said tap delay line circuitry.

16. (currently amended) The PLD of claim 15, wherein said tap delay line circuitry further comprises:

~~at least two columns of registers, each column including at least two registers arranged in serial;~~

a multiplexer circuit respectively associated with a register of each said column, said multiplexer circuit operative to select one of at least two input signals being applied to said multiplexer circuit for application to said associated register, one of said input signals being one of

said plurality of multi-channel signals, and another one of said input signals being the output signal of a register that is conveyed by a tap delay line from a register in a column different than the column said multiplexer circuit applies said input signal to.

17. (original) The DSP circuitry of claim 16, wherein said associated register is a leading register in each said column.

18. (original) The DSP circuitry of claim 16, wherein the output signal of the register being conveyed by the tap delay line is the output of a trailing register in each said column.

19. (original) The DSP circuitry of claim 16, wherein the tap delay line conveys an output signal of a register that is being provided to a first tap to a multiplexer circuit associated with a column that provides an output signal to a second tap.

20. (original) The DSP circuitry of claim 15, wherein said utilization circuitry selectively operates on signals output by a register in each said column.

21. (currently amended) The DSP circuitry of claim 16, further comprising bypass circuitry for enabling the

selected input signal to be routed directly to any one of said ~~at least two~~ registers in said column of registers.

22. (currently amended) The circuitry of claim 1, wherein the interconnection circuitry comprises:

a first multiplexer circuit associated with a first register in [[a]] the first of said columns; and

a second multiplexer circuit associated with a second register in the first column;

wherein each of the first and second multiplexer circuits is operative to select between a same first value and a different second value for application to the respective first and second registers, wherein the same first value is the value at the input of the first column and the different second value is an output from a register that precedes the first and second registers respectively in the first column.

23. (previously presented) The circuitry of claim 22, wherein the first and second multiplexer circuits each comprises a respective first and a respective second input, wherein:

the respective first inputs of the first and second multiplexer circuits are coupled to each other and to the input of the first column; and

the register that precedes the second register in the first column is the first register wherein the second input of the second multiplexer is coupled to the output of the first register.

24. (previously presented) The PLD of claim 15, wherein the interconnection circuitry comprises:

a first multiplexer circuit associated with a first register of said registers in said tap delay line circuitry; and

a second multiplexer circuit associated with a second register of said registers in said tap delay line circuitry;

wherein each of the first and second multiplexer circuits is operative to select between a same first value and a different second value for application to the respective first and second registers, wherein the same first value is the value received at the input of the tap delay line circuitry and the different second value is an output from a register that precedes the respective first and second registers in the tap delay line circuitry.

25. (previously presented) The PLD of claim 24, wherein the first and second multiplexer circuits each comprises a respective first and a respective second input, wherein:

the respective first inputs of the first and second multiplexer circuits are coupled to each other and to the input of the tap delay line circuitry; and

the register that precedes the second register in the tap delay line circuitry is the first register

wherein the second input of the second multiplexer is coupled to the output of the first register.

26. (new) The circuitry of claim 1, wherein the interconnection circuitry:

allows a second channel of said plurality of multi-channel data signals to be selectively shifted, at the same time, through said plurality of registers in a third and a fourth of said columns; and

allows the output of the third column to be selectively shifted through said plurality of registers in the fourth column instead of the second channel that is received by the third and fourth columns at the same time.

27. (new) The circuitry of claim 15, wherein the tap delay line circuitry further comprises:

third and fourth columns of registers for selectively registering, at the same time, the same data of a second of the multiple channels; and

wherein the interconnection circuitry allows an output of the third column to be selectively registered in said plurality of registers in the fourth column instead of the data of the second channel that is received by the third and fourth columns at the same time.